



Patent

Group Art: 1722

# Attorney Docket # 5367-219PUS

# IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of

Volker HÄRLE et al.

Serial No.:

10/566,521

Filed: September 25, 2006

For:

Method for the Production of a Plurality of

Opto-Electronic Semiconductor Chips and Opto-

Electronic Semiconductor Chip

REQUEST FOR CORRECTION OF FILING RECEIPT

Commissioner for Patents P.O. Box 1450 Alexandria, VA 22313-1450

SIR:

Attached is a copy of the official filing receipt received from the U.S. Patent and

Trademark Office in the above-identified application.

There is an error in:

	Applicants' name and/or address
	Title
0	Filing Date
	Serial Number
	Priority Data (country, number)
[x]	Incorrect Priority Date
	Other [pls specify]

which should read as follows: **GERMANY 103 35 081.0 07/31/2003** 

Attorney Docket # 5367-219PUS

A copy of the filing receipt is submitted herewith on which the requested change is entered in red. We have also enclosed a copy of the PCT publication for your viewing upon correction.

It is respectfully requested that a corrected filing receipt be issued.

Respectfully submitted, COHEN PONTANI LIEBERMAN & PAVANE LLP

By:

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Dated: August 6, 2007



## United States Patent and Trademark Office

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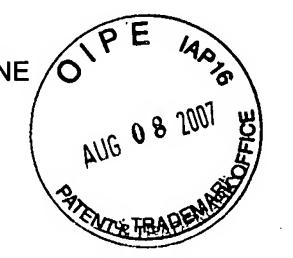
FILING OR 371(c) **TÓT CLMS** ATTY DOCKET NO IND CLMS **ART UNIT** FIL FEE REC'D APPL NO. DATE 18 1030 5367-219PUS 09/25/2006 1722 10/566,521

**CONFIRMATION NO. 7206** 

**FILING RECEIPT** 

\*OC000000023705260\*

27799 COHEN, PONTANI, LIEBERMAN & PAVANE 551 FIFTH AVENUE **SUITE 1210** NEW YORK, NY 10176



Date Mailed: 05/07/2007

Receipt is acknowledged of this regular Patent Application. It will be considered in its order and you will be notified as to the results of the examination. Be sure to provide the U.S. APPLICATION NUMBER, FILING DATE, NAME OF APPLICANT, and TITLE OF INVENTION when inquiring about this application. Fees transmitted by check or draft are subject to collection. Please verify the accuracy of the data presented on this receipt. If an error is noted on this Filing Receipt, please mail to the Commissioner for Patents P.O. Box 1450 Alexandria Va 22313-1450. Please provide a copy of this Filing Receipt with the changes noted thereon. If you received a "Notice to File Missing Parts" for this application, please submit any corrections to this Filing Receipt with your reply to the Notice. When the USPTO processes the reply to the Notice, the USPTO will generate another Filing Receipt incorporating the requested corrections (if appropriate).

Applicant(s)

Volker Harle, Waldetzenberg, GERMANY;

Power of Attorney: The patent practitioners associated with Customer Number 27799.

Domestic Priority data as claimed by applicant

This application is a 371 of PCT/DE04/01594 07/22/2004

**Foreign Applications** 

GERMANY 103 35 081.0 07/30/2003 - 731 2003

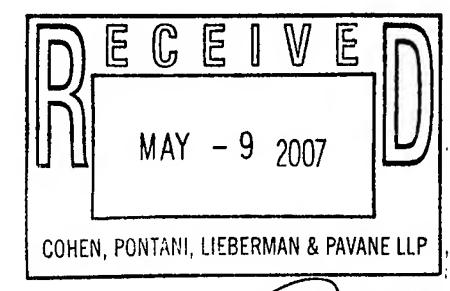
If Required, Foreign Filing License Granted: 05/04/2007

The country code and number of your priority application, to be used for filing abroad under the Paris Convention, is **US10/566,521** 

**Projected Publication Date:** 08/16/2007

Non-Publication Request: No

Early Publication Request: No



#### **Title**

Method for the production of a plurality of opto-electronic semiconductor chips and opto-electronic semiconductor chip

### **Preliminary Class**

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12) NACH DEM VERTRAG ÜBER DIE INTERNATIONALE ZUSAMMENARBEIT AUF DEM GEBIET DES
PATENTWESENS (PCT) VERÖFFENTLICHTE INTERNATIONALE AND AND A SERVICE AND A SER

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**PCT** 

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H01L 21/20,

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(21) Internationales Aktenzeichen:

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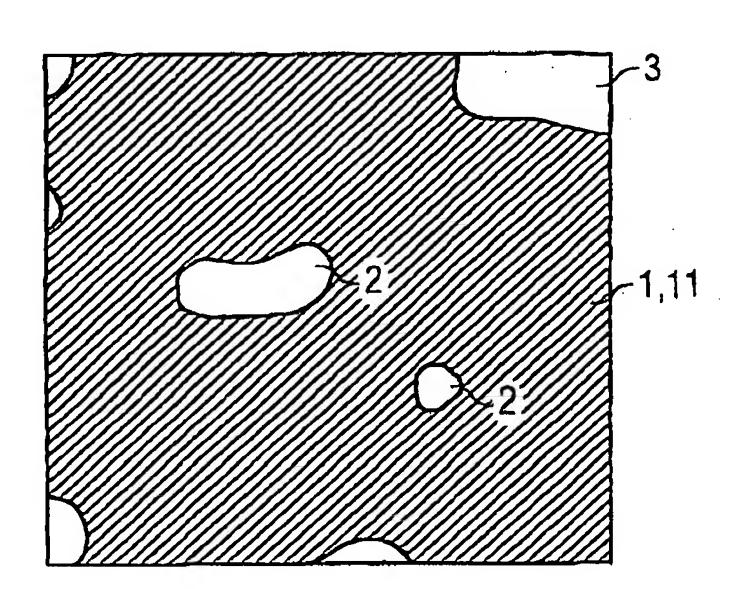
80339 München (DE).

[Fortsetzung auf der nächsten Seite]

(30) Angaben zur Priorität: 31, Juli 2003 (31,07,2003) 103 35 081.0 DE V

(54) Title: METHOD FOR THE PRODUCTION OF A PLURALITY OF OPTO-ELECTRONIC SEMICONDUCTOR CHIPS AND OPTO-ELECTRONIC SEMICONDUCTOR CHIP

(54) Bezeichnung: VERFAHREN ZUR HERSTELLUNG EINER VIELZAHL VON OPTOELEKTRONISCHEN HALBLEITER- 🗸 CHIPS UND OPTOBLEKTRONISCHER HALBLEITERCHIP



(57) Abstract: The invention relates to a method for the production of a plurality of opto-electronic semiconductor chips respectively comprising a plurality of structural elements respectively consisting of at least one semiconductor layer. According to the inventive method, a chip composite base is produced, said base comprising a substrate and an epitaxial surface. A non-closed mask material layer is grown on the epitaxial surface. The mask material layer consists of a plurality of statistically distributed windows having various forms and/or opening surfaces. A masking material is selected in such a way that a semiconductor material of the semiconductor layer, which is grown in a later step of the inventive method, cannot grow on said material or grows in a substantially worse manner in comparison with the epitaxial surface. Subsequently, semiconductor layers are deposited on the epitaxial surface in an essentially simultaneous manner on areas located inside the windows. In another step of the inventive method, the chip composite base with deposited material is separated to form semiconductor chips. The

invention also relates to an optoelectronic semiconductor element produced according to said method.

(57) Zusammensassung: Die Ersindung betrifft ein Verfahren zur Herstellung einer Vielzahl von optoelektronischen Halbleiterchips, die jeweils eine Vielzahl von Strukturelementen mit jeweils mindestens einer Halbleiterschicht aufweisen. Bei dem Verfahren wird eine Chipverbund-Basis bereitgestellt, die ein Substrat sowie eine Aufwachsoberfläche aufweist. Auf die Aufwachsoberfläche wird eine nicht geschlossene Maskenmaterialschicht derart aufgewachsen, dass die Maskenmaterialschicht eine Vielzahl statistisch verteilter Penster mit variierenden Formen und/oder Öffnungsflüchen aufweist, wobei ein Maskenmaterial derart gewählt ist, dass sich ein in einem späteren Verfahrensschritt aufzuwachsendes Halbleitermaterial der Halbleiterschicht auf diesem im Wesentlichen nicht oder im Vergleich zur Aufwachsoberstäche wesentlich schlechter aufwachsen lüsst.

[Fortsetzung auf der nächsten Seite]